A 0.8-WATT, KA-BAND POWER AMPLIFIER

J.M. Schellenberg*, K.L. Tan, R.W. Chan, C.H. Chen
T.S. Lin, D.C. Streit and P.H. Liu

*Schellenberg Associates, Huntington Beach, CA 92647

TRW Inc.
One Space Park, Redondo Beach, CA 90278

ABSTRACT

A hybrid, 2-stage, HEMT power amplifier is reported operating over the 32 to 35 GHz band with a minimum output power of 28 dBm. At 34 GHz, an output power of 0.8 watt with an associated power-added efficiency of 26.6 percent has been demonstrated. Biased for efficiency, this amplifier has demonstrated a power added efficiency of 32.2 percent with an output power of over 0.7 watt.

INTRODUCTION

While multistage amplifiers have been demonstrated at Ka/Q-band frequencies (27 to 50 GHz) with power levels of 0.5 to 0.6 watt, the efficiency in general has been poor, typically less than 15 percent [1-5]. Recent advances have resulted in hybrid and MMIC amplifiers with higher efficiencies, but the output power is typically less than 0.25 watt [6-9].

It is the purpose of this paper to report a 2-stage power amplifier, operating at 34 GHz, with an output power of 29 dBm (0.8 watt) and an associated efficiency of 26.6 percent. This represents the highest reported combination of output power and efficiency for a multistage amplifier operating at these frequencies.

DEVICE DESCRIPTION

The pseudomorphic InGaAs HEMT device structure, shown in Figure 1, was used for this work. The device profile is a double heterojunction HEMT grown by molecular beam epitaxy. Silicon planar doping is employed on both heterojunctions to provide carriers to the InGaAs channel. At 300^{o} K, the 2-dimensional electron sheet charge density, measured on the calibration wafer, was 2.84×10^{12} cm^{-2} with a mobility of 4060 $cm^2/V\text{-}s$.

The device configuration is shown in Figure 2. It consists of eight, 0.25 x 75 µm gate fingers for a total gate periphery

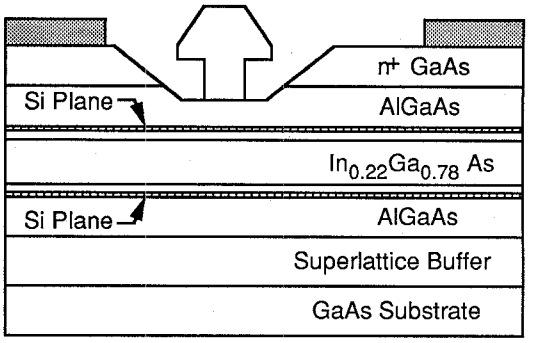

Figure 1. Device cross-section of double heterojunction power InGaAs HEMT.

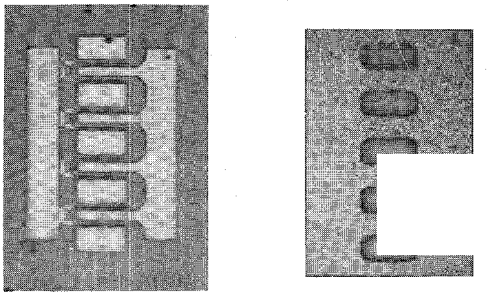

Figure 2. Top and bottom view of 0.6 mm power HEMT.

of 600 µm per chip. Using reactive ion etching (RIE) techniques, small vias are etched into every source pad. In addition to providing a low source inductance, this also serves to provide thermal isolation between the adjacent gate fingers. The chips are thinned to 30 µm, and the back metal is plated to 10 µm thick for low thermal resistance.

Typically, these devices have a full channel current (I_{MAX}) of greater than 600 mA/mm at a gate and drain bias of 0.8 volts and 2 volts, respectively. The average

device transconductance is 506 mS/mm while the average f_T and f_{MAX} is 52.7 GHz and 110 GHz, respectively. Due to the use of undoped AlGaAs, the gate-drain breakdown voltage (defined at 100 μA/mm) is greater than 10 volts. This excellent device breakdown voltage together with the high current density and the high device gain result in measured device power-added efficiencies of typically 40% at 35 GHz.

AMPLIFIER DESIGN

The schematic diagram of the 2-stage power amplifier is shown in Figure 3. It consists of a single 600 μm device driving two 600 μm devices. The two 600 μm devices in the output network are combined using an in-phase combiner/divider network which simultaneously combines and matches the two devices.

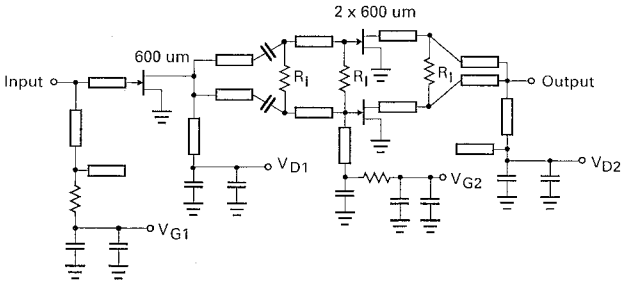

Figure 3. Ka-band, 2-stage power amplifier configuration.

This circuit topology was chosen for simplicity and ease of tuning. Because of the difficulty of realizing reliable low parasitic grounds in hybrid MICs and the difficulty of tuning grounded matching elements, shunt matching elements were purposely avoided in this design. Instead, a design consisting of a cascade of transmission line elements was selected. Specifically, the input network consists of a quarter-wave impedance transformer and the series gate lead inductance. The interstage network consists of a two-section cascade of quarter-wave transmission lines that simultaneously divides the power from the driver and matches the driver output impedance to the input impedance of the output stage. Similarly, the output network, composed of a two-section cascade of quarter-wave transmission lines, combines the power of the two output devices and provides a large-signal match. The isolation resistors, labeled R_I in the figure, are selected to terminate the odd mode.

The bias and bias decoupling networks are also integrated on the carrier and are designed to be independent of the matching networks. This avoids interaction between the bias and matching networks. As shown in the schematic, the bias network consists of a high impedance quarter-wave transmission line with an open circuit low impedance quarter-wave line or capacitor serving as an RF short circuit. In addition, two decoupling capacitor (18 pf and 4700 pf) are included at the edge of the substrate in order to suppress low frequency oscillations. Stabilizing resistors are also included in the gate bias networks to prevent low frequency oscillations.

This 2-stage amplifier circuit, shown in Figure 4, was fabricated with 5 mil thick alumina substrates on a gold plated copper carrier. The overall dimensions of the carrier, including all the bias decoupling capacitors and stabilizing resistors, are 231 x 215 mils.

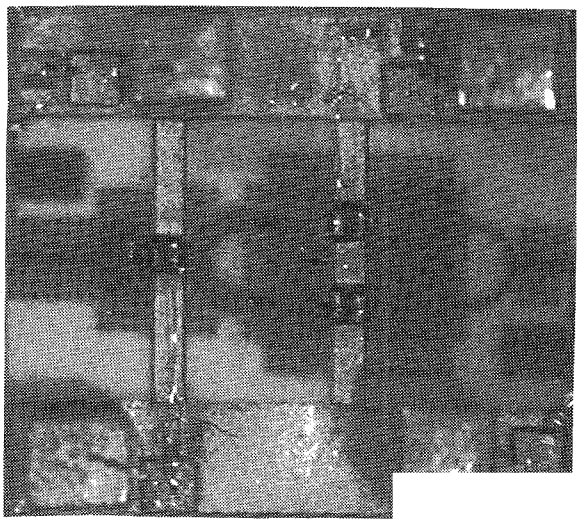

Figure 4. 2-stage power [illegible] assembly.

AMPLIFIER PERFORMANCE

The performance of this 2-stage power amplifier is shown in Figures 5 and 6. These results have been corrected for the loss (0.5 dB at each end) of the input/output waveguide-to-microstrip transitions. Over 20 amplifiers have been tested to date with similar results from all the units, indicating the excellent repeatability of this approach. Figure 5 illustrates the output power versus frequency for two fixed input power levels, 10 dBm and 17 dBm. For this data, the amplifier was biased with $V_{D1} = V_{D2} = 5.5$ volts and $V_G = -0.2$. Only minimal tuning was used to obtain these results. With an input power of 17 dBm, the output power is typically greater than 28 dBm from 32 to 35 GHz.

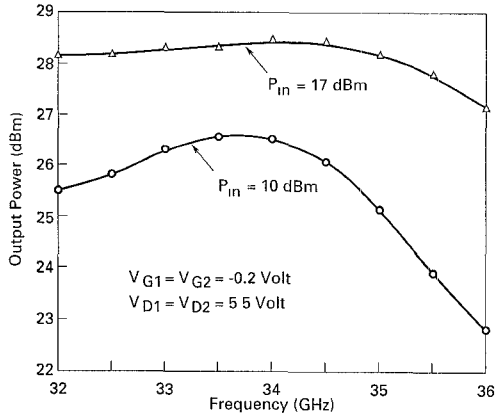

Figure 5. Frequency performance of 2-stage power amplifier.

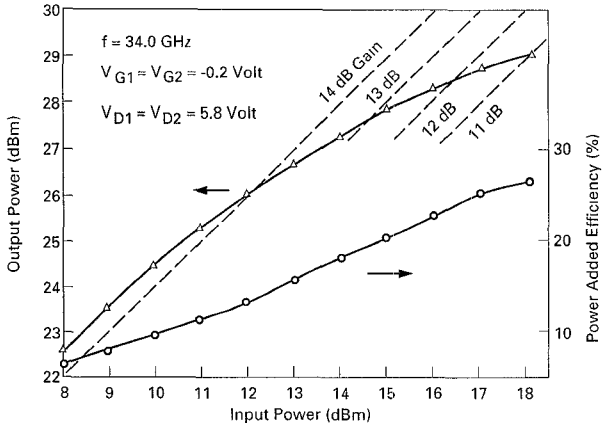

Figure 6. Power performance of 2-stage power amplifier.

Figure 6 illustrates the output power as a function of the input power at a frequency of 34 GHz. Biased at 5.8 volts, this amplifier yielded an output power of 29.0 dBm (0.8 watt) for an input power of 18 dBm. The power-added efficiency is 26.6% at this point. A different unit, biased for maximum efficiency at 5.4 volts, demonstrated a power-added efficiency of 32.2% with an output power of 0.73 watt.

CONCLUSION

The above results represent new levels of performance for FET power amplifiers operating at Ka-band frequencies. These results together with recently reported Ka/Q-band power amplifier results (both hybrid and monolithic) are summarized in Table 1 for comparison. While comparable power and efficiency levels have been separately reported, until now, no one has simultaneously achieved both high power (0.8 watt) and reasonable efficiencies (greater than 20%). The results reported in this paper clearly represent a significant advance in Ka-band power amplifiers. Further, these results were achieved with minimal tuning in a single design iteration.

ACKNOWLEDGMENT

The authors would like to thank R. Dia for wafer processing, L. Callejo for amplifier assembly and test, members of the MBE and EBL groups for their outstanding support and S. K. Wang for his technical contribution and support.

Table 1. Ka/Q-Band, Multistage Power Amplifier Results

Ref.	Freq. (GHz)	Max. Pwr. (Watt)	Assc. Gain (dB)	BW(1-dB) (GHz)	PA Eff. (%)	Type
This work	34	0.8*	11	>3	26.6	Hybrid
This work	34.5	0.73	14	>3	32.2*	Hybrid
[1]	42	0.5	7	1	7	Hybrid
[2]	50	0.6	18	2	5	Hybrid
[3]	28	0.56	7.2	1	15	MMIC
[4]	44	0.25	8	3	11	MMIC
[5]	47	0.5	10	1	5	Hybrid
[6]	34	0.11	16	-	21.6	MMIC
[7]	32	0.09	14	-	25.9	MMIC
[8]	44	0.25	13.6	3	26.8	Hybrid
[9]	36	0.22	20	4	21.5	MMIC

*Optimized Parameter

REFERENCES

[1] G. Hegazi, H-L. A. Hung, J. L. Singer, F. R. Phelleps, A. B. Cornfeld, T. Smith, J. F. Bass, H. E. Carlson and H. C. Huang, "GaAs Molecular Beam Epitaxy Monolithic Power Amplifiers at U-Band," 1989 IEEE MTT-S Digest, pp. 209-213, June 1989.

[2] N. Camilleri, P. Chye and R. Prioriello, "Monolithic 50 GHz GaAs FET Power Amplifier," Technical Digest, 1989 IEEE GaAs IC Symposium, pp. 267-270, October 1989.

[3] Y. Oda, T. Yoshida, K. Kai, S. Arai and S. Yanagawa, "Ka-Band Monolithic GaAs Two-Stage Power Amplifier," 1989 IEEE Monolithic Circuits Sym. Digest, pp. 33-36, June 1989.

[4] H. Yang, R. M. Herman, K. W. Angel, A. M. Chao, M. J. Schindler, M. Adlerstein, Y. Tajima and D. M. Danzilio, "A 0.25-Watt Three-Stage Q-Band MESFET Monolithic Power Amplifier," Technical Digest, 1991 IEEE GaAs IC Symposium, pp. 161-164, October 1991.

[5] G. Hegazi, K. Pande, F. Phelleps, E. Chang, A. Cornfeld, P. Rice, M. Ghahremeni and P. Pages, "A 0.5-Watt 47-GHz Power Amplifier Using GaAs Monolithic Circuits," IEEE Microwave & Guided Wave Lett., vol. 2, pp. 61-62, February 1992.

[6] P. Saunier, H. Q. Tserng, N. Camilleri, K. Bradshaw and H. D. Shih, "A High Efficiency Ka-Band Monolithic GaAs FET Amplifier," Technical Digest, 1988 IEEE GaAs IC Symposium, pp. 37-39, November 1988.

[7] P. Saunier, et. al, "Doped-Channel Heterojunction Structures for Millimeter-Wave Discrete Devices and MMICs," MILCOM 1989 Digest of Papers, pp. 730-734, May 1989.

[8] D. W. Ferguson, P. M. Smith, P. C. Chao, L. F. Lester, R. P. Smith, P. Ho, A. Jabra and J. M. Ballingall, "44 GHz Hybrid HEMT Power Amplifiers," 1989 IEEE MTT-S Digest, pp. 987-990, June 1989.

[9] D. W. Ferguson, S. A. Allen, M. Y. Kao, P. M. Smith, P. C. Chao, M. A. G. Upton and J. M. Ballingall, "35 GHz Pseudomorphic HEMT MMIC Power Amplifier," 1991 IEEE MTT-S Digest, pp. 335-338, June 1991.